WHAT IS CLAIMED IS:

1. An interrupt control apparatus having a function of normal interrupt and a function of break-interrupt, said apparatus comprising:

a first information holding section for holding, at the time of a normal interrupt, operation information of a processor before said normal interrupt;

a second information holding section for holding, at the time of a break-interrupt, operation information of said processor before said break-interrupt;

a return operation specifying section for specifying whether a return operation from a normal interrupt state or a return operation from a break-interrupt state is to be performed in returning from an interrupt operation; and

an interrupt return section for re-setting operation information held in said first information holding section or operation information held in said second information holding section in accordance with operation contents specified by said return operation specifying section, and thereby returning the state of said processor from an interrupt operation state to a state before the interrupt.

2. An apparatus according to claim 1, wherein said second information holding section holds an instruction address before the break-interrupt, to

which said processor is to return from the break-interrupt operation state.

3. An apparatus according to claim 2, wherein said second information holding section further holds the processor state before the break-interrupt.

4. An apparatus according to claim 2, wherein said second information holding section further holds a factor of the break-interrupt.

5. An apparatus according to claim 2, wherein said second information holding section further holds the processor state before the break-interrupt and a factor of the break-interrupt.

6. An apparatus according to claim 1, wherein said return operation specifying section specifies the return operation using flag information which is set at the time of interrupt and shows whether the interrupt is the break-interrupt or not.

7. An apparatus according to claim 1, wherein said return operation specifying section specifies the return operation in accordance with a value described in an operand of an interrupt return instruction.

8. An apparatus according to claim 1, wherein said return operation specifying section specifies the return operation in accordance with contents of an instruction field of an interrupt return instruction.

9. An interrupt control method comprising the

steps of:

when a normal interrupt occurs, holding operation information of a processor before said normal interrupt in a first information holding section;

when a break-interrupt occurs, holding operation information of said processor before said break-interrupt in a second information holding section different from said first information holding section, and setting a flag for showing whether or not the break-interrupt state is set, to the break-interrupt state; and

in returning said processor from the interrupt state to a state before the interrupt, selecting and restoring one of operation information in said first information holding section and operation information in said second information holding section in accordance with a value of said flag.

10. An interrupt control method comprising the steps of:

when a normal interrupt occurs, holding operation information of a processor before said normal interrupt in a first information holding section;

when a break-interrupt occurs, holding operation information of said processor before said break-interrupt in a second information holding section different from said first information holding

section; and

in returning said processor from the interrupt state to a state before the interrupt, selecting and restoring one of operation information in said first information holding section and operation information in said second information holding section in accordance with contents of an interrupt return instruction.

11. An interrupt control method for an interrupt control apparatus having a function of normal interrupt and a function of break-interrupt, said method comprising the steps of:

when a break-interrupt occurs, holding at least an instruction address before said break-interrupt, to which a processor is to return from a break-interrupt state, and setting a flag for representing whether or not said break-interrupt state is set, to said break-interrupt state; and

in returning said processor from said break-interrupt state to a state before said break-interrupt, canceling said flag for representing said break-interrupt state, and restoring said instruction address which has been held.

12. A method according to claim 11, further comprising the steps of:

when said break-interrupt occurs, holding not only said instruction address but also the processor state before said break-interrupt, and

in returning said processor from said break-interrupt state to said state before said break-interrupt, restoring said processor state, which has been held.

13. A method according to claim 11, further comprising the step of:

when said break-interrupt occurs, holding not only said instruction address but also a factor of said break-interrupt.

14. An interrupt control apparatus applied to a data processing system having a function of executing a conditional instruction, said apparatus comprising:

a break detection section for detecting a breakpoint set at an arbitrary position of an instruction sequence;

a condition determination section for determining whether or not a condition of said conditional instruction is satisfied; and

a control section for controlling a break-interrupt on the basis of a breakpoint detection result from said break detection section and a determination result from said condition determination section.

15. An interrupt control apparatus applied to a data processing system having a function of executing a conditional instruction, said apparatus comprising:

an instruction break detection section for detecting an instruction break in accordance with

whether or not an instruction corresponding to an instruction address representing a breakpoint, which is set in a register, is read out, and outputting a detection signal representing a detection result;

a condition determination section for determining whether or not a condition of the read-out conditional instruction is satisfied, and outputting a determination signal representing a determination result; and

a logical operation section for performing AND operation to said detection signal output from said instruction break detection section and said determination signal output from said condition determination section, and sending a break-interrupt notification in accordance with the AND operation result.

16. An apparatus according to claim 15, wherein

said condition determination section is designed to determine whether or not an instruction word is said conditional instruction, if said instruction word is said conditional instruction, determine whether or not the condition is satisfied, and output the determination signal representing the result, and

when an instruction word corresponding to the instruction address representing said breakpoint is an unconditional instruction or a conditional instruction having an unsatisfied condition, said logical operation section does not send a

break-interrupt notification, and when said instruction word is the conditional instruction having a satisfied condition, said logical operation section sends said break-interrupt notification.

17. An apparatus according to claim 15, wherein said apparatus further comprises a mode setting section for setting one of a first mode in which said break-interrupt is generated when a generation condition of said instruction break is satisfied, and the condition of said conditional instruction is satisfied, and a second mode in which said break-interrupt is generated when said generation condition of said instruction break is satisfied,

said condition determination section is designed to determine whether or not an instruction word is said conditional instruction, if said instruction word is said conditional instruction, determine whether or not the condition is satisfied, and output the determination signal representing the result, and

in said first mode, when an instruction word corresponding to the instruction address representing said breakpoint is an unconditional instruction or a conditional instruction having an unsatisfied condition, said logical operation section does not sends a break-interrupt notification, and when said instruction word is the conditional instruction having a satisfied condition, said logical operation section sends a break-interrupt notification, and in

said second mode, when said instruction word is an instruction word corresponding to the instruction address representing said breakpoint, said logical operation section sends said break-interrupt notification.

18. An apparatus according to claim 15, wherein said condition determination section is designed to determine whether or not an instruction word is said conditional instruction, if said instruction word is said conditional instruction, determine whether or not the condition is satisfied, and output the determination signal representing the result, and when an instruction word corresponding to the instruction address representing said breakpoint is a conditional instruction having an unsatisfied condition, said logical operation section does not send a break-interrupt notification, and when said instruction word is an unconditional instruction or the conditional instruction having a satisfied condition, said logical operation section sends said break-interrupt notification.

19. An apparatus according to claim 15, wherein said apparatus further comprises a mode setting section for setting one of a first mode in which said break-interrupt is generated when a generation condition of said instruction break is satisfied, and the condition of said conditional instruction is satisfied, and a second mode in which said

break-interrupt is generating when said generation condition of said instruction break is satisfied,

said condition determination section is designed to determine whether or not an instruction word is said conditional instruction, if said instruction word is said conditional instruction, determine whether or not the condition is satisfied, and output the determination signal representing the result, and

in said first mode, when an instruction word corresponding to the instruction address representing said breakpoint is a conditional instruction having an unsatisfied condition, said logical operation section does not send a break-interrupt notification, and when said instruction word is an unconditional instruction or the conditional instruction having a satisfied condition, said logical operation section sends a break-interrupt notification, and in said second mode, when said instruction word is an instruction word corresponding to the instruction address representing said breakpoint, said logical operation section sends said break-interrupt notification.

20. An apparatus according to claim 15, wherein said data processing system comprises one of a scalar processor for performing one unit of processing in accordance with one instruction, a long instruction word processor for parallelly executing short instructions forming a long instruction word, and a

parallel processor for parallelly executing at least one basic instruction forming a variable-length instruction word.

21. An interrupt control apparatus applied to a data processing system having a function of executing a conditional instruction, said apparatus comprising:

an instruction break detection section for detecting an instruction break in accordance with whether or not an instruction corresponding to an instruction address representing a breakpoint, which is set in a register, is read out, and sending a break-interrupt notification in accordance with a detection result; and

a control section for, in an interrupt handler activated in accordance with said break-interrupt notification supplied from said instruction break detection section, determining whether or not a condition of said conditional instruction is satisfied, and controlling break-interrupt processing in accordance with a determination result.

22. An apparatus according to claim 21, wherein said control section determines, in said interrupt handler, whether or not an instruction word as an instruction break target is said conditional instruction, when said instruction word is said conditional instruction, determines whether or not a condition of said conditional instruction is satisfied, when said instruction word as said

instruction break target is an unconditional instruction or a conditional instruction having an unsatisfied condition, returns from said interrupt handler, and when said instruction word as said instruction break target is a conditional instruction having a satisfied condition, performs said break-interrupt processing.

23. An apparatus according to claim 21, wherein said apparatus further comprises a mode setting section for setting one of a first mode in which said break-interrupt is generated when a generation condition of said instruction break is satisfied, and the condition of said conditional instruction is satisfied, and a second mode in which said break-interrupt is generated when said generation condition of said instruction break is satisfied, and

in said first mode, said control section determines, in said interrupt handler, whether or not an instruction word as an instruction break target is said conditional instruction, when said instruction word is said conditional instruction, determines whether or not a condition of said conditional instruction is satisfied, when said instruction word as said instruction break target is an unconditional instruction or a conditional instruction having an unsatisfied condition, returns from said interrupt handler, and when said instruction word as said instruction break target is a conditional instruction

having a satisfied condition, performs said break-interrupt processing, and in said second mode, said control section performs said break-interrupt processing when receiving said break-interrupt notification.

24. An apparatus according to claim 21, wherein said control section determines, in said interrupt handler, whether or not an instruction word as an instruction break target is said conditional instruction, when said instruction word is said conditional instruction, determines whether a condition of said conditional instruction is satisfied, when said instruction word as said instruction break target is a conditional instruction having an unsatisfied condition, returns from said interrupt handler, and when said instruction word as said instruction break target is an unconditional instruction or a conditional instruction having a satisfied condition, performs said break-interrupt processing.

25. An apparatus according to claim 21, wherein said apparatus further comprises a mode setting section for setting one of a first mode in which said break-interrupt is generated when a generation condition of said instruction break is satisfied, and the condition of said conditional instruction is satisfied, and a second mode in which said break-interrupt is generated when said generation

condition of said instruction break is satisfied, and

in said first mode, said control section determines, in said interrupt handler, whether or not an instruction word as an instruction break target is said conditional instruction, when said instruction word is said conditional instruction, determines whether or not a condition of said conditional instruction is satisfied, when said instruction word as said instruction break target is a conditional instruction having an unsatisfied condition, returns from said interrupt handler, and when said instruction word as said instruction break target is an unconditional instruction or a conditional instruction having a satisfied condition, performs said break-interrupt processing, and in said second mode, said control section performs said break-interrupt processing when receiving said break-interrupt notification.

26. An apparatus according to claim 21, wherein said data processing system comprises one of a scalar processor for performing one unit of processing in accordance with one instruction, a long instruction word processor for parallelly executing short instructions forming a long instruction word, and a parallel processor for parallelly executing at least one basic instruction forming a variable-length instruction word.

27. An interrupt control apparatus applied to a

data processing system having a function of executing a conditional instruction, said apparatus comprising:

a software break detection section for detecting a software break in accordance with whether or not a breakpoint instruction replaced at an arbitrary position of an instruction sequence is executed, and sending a break-interrupt notification in accordance with a detection result; and

a control section for, in an interrupt handler activated in accordance with said break-interrupt notification supplied from said software break detection section, determining whether or not a condition of said conditional instruction is satisfied, and controlling break-interrupt processing in accordance with a determination result.

28. An apparatus according to claim 27, wherein said control section determines, in said interrupt handler, whether or not an instruction word as a software break target is said conditional instruction, when said instruction word is said conditional instruction, determines whether or not a condition of said conditional instruction is satisfied, when said instruction word as said software break target is an unconditional instruction or a conditional instruction having an unsatisfied condition, returns from said interrupt handler, and when said instruction word as said software break target is a conditional instruction having a satisfied condition,

performs said break-interrupt processing.

29. An apparatus according to claim 27, wherein said apparatus further comprises a mode setting section for setting one of a first mode in which said break-interrupt is generated when a generation condition of said software break is satisfied, and the condition of said conditional instruction is satisfied, and a second mode in which said break-interrupt is generating when said generation condition of said software break is satisfied, and

in said first mode, said control section determines, in said interrupt handler, whether or not an instruction word as a software break target is said conditional instruction, when said instruction word is said conditional instruction, determines whether or not a condition of said conditional instruction is satisfied, when said instruction word as said software break target is an unconditional instruction or a conditional instruction having an unsatisfied condition, returns from said interrupt handler, and when said instruction word as said software break target is a conditional instruction having a satisfied condition, performs said break-interrupt processing, and in said second mode, said control section performs said break-interrupt processing when receiving said break-interrupt notification.

30. An apparatus according to claim 27, wherein

said control section determines, in said interrupt handler, whether or not an instruction word as a software break target is said conditional instruction, when said instruction word is said conditional instruction, determines whether or not a condition of said conditional instruction is satisfied, when said instruction word as said software break target is a conditional instruction having an unsatisfied condition, returns from said interrupt handler, and when said instruction word as said software break target is an unconditional instruction or a conditional instruction having a satisfied condition, performs said break-interrupt processing.

31. An apparatus according to claim 27, wherein said apparatus further comprises a mode setting section for setting one of a first mode in which said break-interrupt is generated when a generation condition of said software break is satisfied, and the condition of said conditional instruction is satisfied, and a second mode in which said break-interrupt is generating when said generation condition of said software break is satisfied, and

in said first mode, said control section determines, in said interrupt handler, whether or not an instruction word as a software break target is said conditional instruction, when said instruction word is said conditional instruction, determines whether or not a condition of said conditional

instruction is satisfied, when said instruction word as said software break target is a conditional instruction having an unsatisfied condition, returns from said interrupt handler, and when said instruction word as said software break target is an unconditional instruction or a conditional instruction having a satisfied condition, performs said break-interrupt processing, and in said second mode, said control section performs said break-interrupt processing when receiving said break-interrupt notification.

32. An apparatus according to claim 27, wherein said data processing system comprises one of a scalar processor for performing one unit of processing in accordance with one instruction, a long instruction word processor for parallelly executing short instructions forming a long instruction word, and a parallel processor for parallelly executing at least one basic instruction forming a variable-length instruction word.

33. An interrupt control method for controlling a break-interrupt in a data processing system having a function of executing a conditional instruction, said method comprising the steps of:

detecting a breakpoint set at an arbitrary position of an instruction sequence;

determining whether or not a condition of said conditional instruction is satisfied; and

controlling the break-interrupt on the basis of a detection result of said breakpoint and a determination result of said conditional instruction.